CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A sigma delta converter comprising:

[[an]] integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component;

a pair of capacitors coupled to the integrator input;

a first set of switches coupled to the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage; and

a second set of switches coupled between the pair of capacitors and the integrator input, the second set of switches configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase.

2. (Previously Presented) The sigma delta converter, as recited in Claim 1, further comprising:

a comparator coupled to the integrator circuitry output, the comparator including a comparator output.

3. (Previously Presented) The sigma delta converter, as recited in Claim 1, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta loop filter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output.

4. (Previously Presented) The sigma delta converter, as recited in Claim 1, further comprising:

a comparator coupled to the integrator circuitry output, the comparator including a comparator output;

a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output; and

a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output, wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal.

5. (Previously Presented) The sigma delta converter, as recited in Claim 1, further comprising:

a digital to analog converter coupled to the pair of capacitors for producing the second charge.

6. (Previously Presented) The sigma delta converter, as recited in Claim 5, the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor.

7. (Previously Presented) The sigma delta converter, as recited in Claim 1, wherein the integrator is a continuous time integrator.

8. (Previously Presented) The sigma delta converter, as recited in Claim 1, wherein the integrator is a discrete time integrator.

9. (Currently Amended) A radio frequency (RF) signal receive path comprising:

an intermediate frequency amplifier (IFA) including an IFA output;

a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs having an AAF output; and

a sigma delta converter coupled to the AAF output, the sigma delta converter comprising:

integrator circuitry including an integrator input and an integrator output, wherein an input signal coupled to the integrator input has an input AC voltage component and a DC offset component;

a pair of capacitors coupled to the integrator input;

a first set of switches coupled to the pair of capacitors, the first set of switches configured to transfer a first charge to the pair of capacitors during a first phase, the first charge proportional to a reference voltage; and

a second set of switches coupled to the pair of capacitors, the second set of switches configured to transfer the first charge and a second charge to the integrator input during a second phase, the second charge proportional to the DC offset component and based on a voltage applied in series with the pair of capacitors during the second phase.

10. (Original) The RF signal receive path, as recited in Claim 9, wherein the integrator circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta converter, each of the N integrators having a first input, a second input, a first output and a second output, each of the N integrators having a first integrator capacitor coupled to the first input and the first output and a second integrator capacitor coupled to the second input and the second output.

11. (Previously Presented) The RF signal receive path, as recited in Claim 9, the sigma delta converter further comprising:

a comparator coupled to the integrator output, the comparator including a comparator output;

a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output; and

a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output, wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal.

12. (Previously Presented) The RF signal receive path, as recited in Claim 9, the sigma delta converter further comprising:

a digital to analog converter coupled to the pair of capacitors for producing the second charge.

13. (Original) The RF signal receive path, as recited in Claim 12, the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor.

14. (Original) The RF signal receive path, as recited in Claim 9, wherein the integrator is a continuous time integrator.

15. (Original) The RF signal receive path, as recited in Claim 9, wherein the integrator is a discrete time integrator.

16. (Currently Amended) A method comprising:

during a first phase, charging a pair of capacitors to a reference charge;

during a second phase, applying a voltage in series with the pair of capacitors to provide a DC offset correction charge; and

during the second phase, transferring a sum charge via the pair of capacitors to inputs of a first integrator in a series of integrators in a sigma delta converter, the sum charge including the reference charge and [[a]]the DC offset correction charge.

17. (Original) The method, as recited in Claim 16, further comprising:

comparing an output of a last integrator in the series of integrators to a zero value; and

determining a polarity of the reference charge in the sum charge based on a result of the comparing.

18. (Original) The method, as recited in Claim 17, wherein a polarity of the DC offset correction charge in the sum charge is independent of a result of the comparing.

19. (New) The sigma delta converter of claim 1, wherein:

the pair of capacitors comprises a first capacitor having a first terminal and a second terminal and a second capacitor having a first terminal and a second terminal;

the first pair of switches comprises:

a first switch comprising a first terminal coupled to a first terminal of a first voltage reference and a second terminal coupled to the first terminal of the first capacitor;

a second switch comprising a first terminal coupled to a second terminal of the first voltage reference and a second terminal coupled to the first terminal of the second capacitor;

a third switch comprising a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to a second voltage reference; and

a fourth switch comprising a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to the second voltage reference; and

the second pair of switches comprises:

a fifth switch comprising a first terminal configured to receive a first voltage based on the DC offset component and a second terminal coupled to the first terminal of the first capacitor;

a sixth switch comprising a first terminal configured to receive a second voltage based on the DC offset component and a second terminal coupled to the first terminal of the second capacitor;

a seventh switch comprising a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to a first terminal of the integrator input; and

an eighth switch comprising a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to a second terminal of the integrator input.

20. (New) The radio frequency (RF) signal receive path of claim 7, wherein:

the pair of capacitors comprises a first capacitor having a first terminal and a second terminal and a second capacitor having a first terminal and a second terminal;

the first pair of switches comprises:

a first switch comprising a first terminal coupled to a first terminal of a first voltage reference and a second terminal coupled to the first terminal of the first capacitor;

a second switch comprising a first terminal coupled to a second terminal of the first voltage reference and a second terminal coupled to the first terminal of the second capacitor;

a third switch comprising a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to a second voltage reference; and

a fourth switch comprising a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to the second voltage reference; and

the second pair of switches comprises:

a fifth switch comprising a first terminal configured to receive a first voltage based on the DC offset component and a second terminal coupled to the first terminal of the first capacitor;

a sixth switch comprising a first terminal configured to receive a second voltage based on the DC offset component and a second terminal coupled to the first terminal of the second capacitor;

a seventh switch comprising a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to a first terminal of the integrator input; and

an eighth switch comprising a first terminal coupled to the second terminal of the second capacitor and a second terminal coupled to a second terminal of the integrator input.